Reg.No.:												

VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN

[AUTONOMOUS INSTITUTION AFFILIATED TO ANNA UNIVERSITY, CHENNAI]

Elayampalayam – 637 205, Tiruchengode, Namakkal Dt., Tamil Nadu.

Question Paper Code: 7024

M.E. / M.Tech. DEGREE END-SEMESTER EXAMINATIONS – JUNE / JULY 2024

Second Semester

VLSI Design

P23VD205 - LOW POWER VLSI DESIGN

(Regulation 2023)

Time: 3:00 Hours Maximum: 100 Marks

Answer ALL the questions

Knowledge Levels (KL)	K1 – Remembering	K3 – Applying	K5 - Evaluating
	K2 – Understanding	K4 – Analyzing	K6 - Creating

PART – A

(10 x 2 = 20 Marks)

Q.No.	Questions	Marks	KL	CO
1.	What are the sources of power consumption in VLSI?	2	K2	CO1
2.	Define Physics of Power Dissipation in CMOS.	2	K6	CO1
3.	What is the concept of low-power design?	2	K1	CO2
4.	What do you mean by circuit level low-power design?	2	K4	CO2
5.	Define Sequential Logic and Combinational Logic.	2	K2	CO3
6.	List various stages of VLSI physical design process.	2	K2	CO3
7.	Define LNS and Power Dissipation.	2	K2	CO4
8.	What is meant by probabilistic analysis?	2	K2	CO4
9.	State the use of Behavioral Level Transform.	2	K1	CO5
10.	Mention the Algorithms used in Low Power Design.	2	K6	CO5

PART – B

(5 x 13 = 65 Marks)

Q.No.		Questions	Marks	KL	CO
11.	a)	Explain the Basic principle of low power design.	13	K5	CO1
		(OR)			
	b)	Explain Systolic Array and Packing Efficiency.	13	K1	CO1
12.	a)	Explain the low power VLSI design concepts at architecture level.	13	K2	CO2
		(OR)			
	b)	Explain in detail about the circuit level Low Power Design Methodology.	13	K2	CO2
13.	a)	Discuss about static and dynamic power dissipation in CMOS circuits.	13	K2	CO3
		(OR)			
	b)	Write short notes on the following.			
		i. Semiconductor memories.	7	K3	CO3
		ii. Placement and Routing.	6	K3	CO3
14.	a)	What is the difference among Circuit Level, Gate Level and Behavioral Level. Explain with suitable examples.	13	K1	CO4
		(OR)			
	b)	What are the various stages of placement in physical design?	13	K2	CO4
15.	a)	Explain in detail about the popular techniques to design low power VLSI circuits?	13	K6	CO5
		(OR)			
	b)	Explain in detail about the synthesis of low power VLSI design.	13	K3	CO5

PART – C

(1 x 15 = 15 Marks)

Q.No.		Questions	Marks	KL	CO
16.	a)	Discuss in detail about strategy used for sequential circuit power estimation?	15	K6	CO5
		(OR)			
	b)	Explain the role of standard cells and rows in floor plans? What is the significance of clock tree and power grid in placement?	15	K6	CO3